Amendments to the Specification:

Please add the following two new paragraphs after paragraph 21:

[Para 21.1] Fig. 8 is a diagram illustrating a reference signal circuit 60 producing reference signals.

[Para 21.2] Fig. 9 is a diagram illustrating a clock generator 62 producing clock signals.

Please replace paragraph 22 with the following amended paragraph:

[Para 22] Please refer to Fig. 5, Fig. 8, and Fig. 9. Fig. 5 ~~, which~~ is a schematic diagram of the switched capacitor circuit 30 of the present invention. Fig. 8 is a diagram illustrating a reference signal circuit 60 producing reference signals. Fig. 9 is a diagram illustrating a clock generator 62 producing clock signals. As shown [[is]] in Fig. 5, the switched capacitor circuit 30 includes an operational amplifier 40, two sampling capacitors 31, 41, two input reset switches 32, 42, two signal input switches 33, 43, two reference input switches 34, 44, two reference reset switches 35, 45, and two feedback networks 36, 46. The switched capacitor circuit 30 further comprises [[a]] the reference signal circuit 60 ~~(not shown)~~ for generating a reference signal V_{REFP}, a reference signal V_{REFN}, and a common signal V_{COM}, and [[a]] the clock generator 62 ~~(not shown)~~ for generating a first clock signal CLK21, a second clock signal CLK22, a third clock signal CLK12, and a clock signal CMP. On the upper side of the switched capacitor circuit 30, the first terminal of the sampling capacitor 31 is connected to the first input terminal of the operational amplifier 40, the first terminal of the input reset switch 32 is also connected to the first input terminal of the operational amplifier 40, the first terminal of the signal input switch 33 is connected to the second terminal of the sampling capacitor 31, the first terminal of the reference input switch 34 is also connected to the second terminal of the sampling capacitor 31, and the first terminal of the reference reset switch 35 is connected to the second terminal of the reference input switch 34. The input signal

V_{IN+} is inputted through the second terminal of signal input switch 33, the reference signal V_{REFP} is inputted through the second terminal of reference input switch 34, and the common signal V_{COM} is inputted through both the second terminal of the input reset switch 32 and the second terminal of the reference reset switch 35. The lower side of the switched capacitor circuit 30 has a similar electrical structure to the upper side.

Please replace paragraph 24 with the following amended paragraph:

[Para 24] Please refer to Fig. 6, which is the schematic diagram of the clock signal in Fig.5. The first clock signal CLK21, the second clock signal CLK22, the third clock signal CLK12 and the clock signal CMP are generated by [[a]] the clock generator 62, wherein the clock signal CLK21 is the opposite of CLK22 with a little phase shift, and the third clock signal CLK12 is an early-falling form of the first clock signal CLK21. The clock signal CMP is utilized by the pipeline ADC 10. When the first clock signal CLK21 is pulled up, the input signal V_{IN} is sampled and transmitted to the sampling capacitors 31, 41, 37, 47, and the operational amplifier 40 is inactive at that moment. When the second clock signal CLK22 is pulled up, the reference signal V_{REF} is also connected to the sampling capacitors 31, 41, so the electrical charge of the sampling capacitors 31, 41 is equal to the difference of the input signal V_{IN} and the reference signal V_{REF}. Then the electrical charge is converted to a corresponding output signal V_{res} through the operational amplifier 40. Referring to Fig. 6 and Fig. 5 at the same time, according to the clock signal in Fig. 6, the method of operating the capacitor switched circuit includes: (a) turning on the reference reset switches 35, 45 after the reference input switches 34, 44 are turned off in order to transmit the common signal V_{COM} to the second terminals of reference input switches 34, 44, then turning on the signal input switches 33, 43 in order to transmit the input signal V_{REFP} to the sampling capacitors 31, 41; (b) turning off the reference reset switches 35, 45, then turning off the signal input switches 33, 43; and (c) turning on the reference input switches 34, 44, after the signal input switches 33, 43 are turned off.

Please replace paragraph 27 with the following amended paragraph:

[Para 27] Please refer to Fig. 7, which is a schematic diagram of the simulated output signal of the prior art switched capacitor circuit [[62]] and the simulated output signal of the switched capacitor circuit of the present invention [[64]] 30, wherein the simulated output signal of the typical switched capacitor circuit [[62]] is drawn as a solid line, and the simulated output signal of the switched capacitor circuit of the present invention [[64]] 30 is drawn as a dotted line. As shown in figure, the simulated output signal of the typical switched capacitor circuit [[62]] shows overshooting when it changes state, because the difference of the reference signal and the input signal is amplified by the operational amplifier, worsening the phenomenon when the input signal swings. Comparing the simulated output signal of the typical switched capacitor circuit [[62]] with the simulated output signal of the switched capacitor circuit of the present invention [[64]] 30, the simulated output signal of the switched capacitor circuit of the present invention [[64]] 30 has smaller overshooting, because the reference signal is forced to the median value then pulled high or low to reduce the overshooting.